

Lithium-Ion/Polymer/Iron Protector
Features

- High accuracy voltage detection circuit
 - Overcharge detection : $\pm 25\text{mV}$
- Low power consumption
 - Supply current: $6.6\mu\text{A}$ max. ($T_a = +25^\circ\text{C}$)
- Delay times of overcharge is generated by an internal circuit (fixed).
- Built-in breaking wire detector function
- Package: 8 pin SOP、20 pin TSSOP、48 pin LQFP
- Lead-free, Sn 100%, Halogen-free

Description

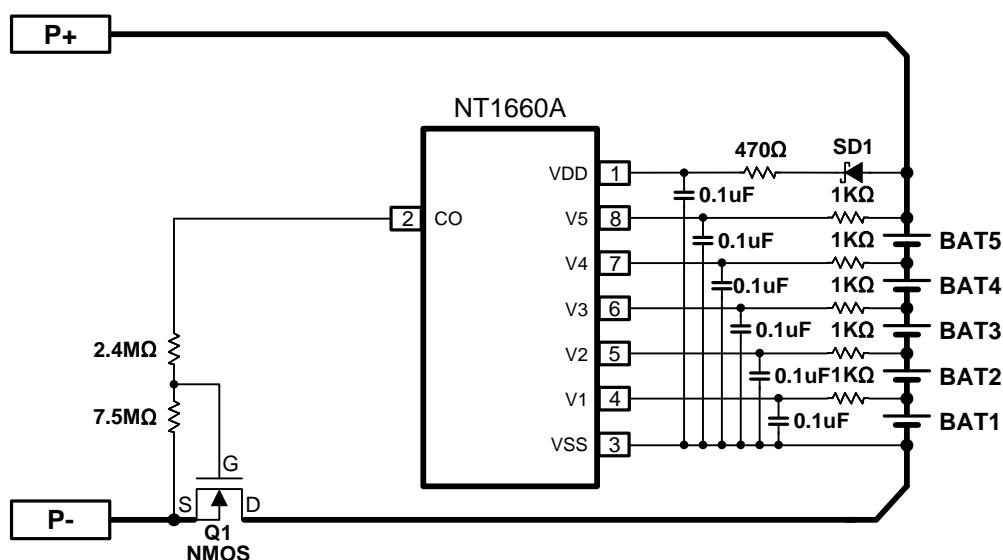
The NT1660/NT1662/NT1663/NT1664 series are the 4~20-cell secondary protection IC for lithium-ion /lithium-polymer /lithium-iron phosphate rechargeable battery pack. The high accuracy voltage detector and delay time circuits are built in NT1660/NT1662/NT1663/NT1664 series with state-of-the-art design and process.

Applications

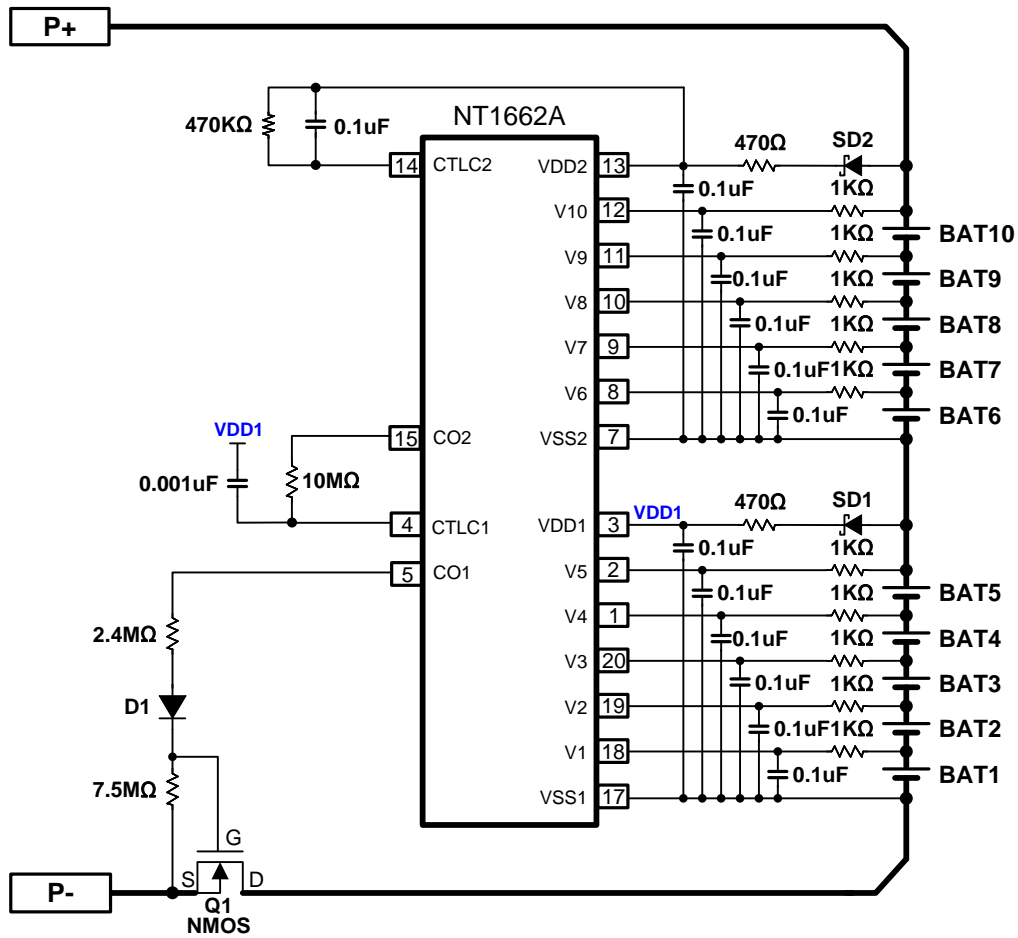
- Lithium-ion rechargeable battery pack
- Lithium-polymer rechargeable battery pack
- Lithium-iron phosphate rechargeable battery pack

Typical Application Circuit

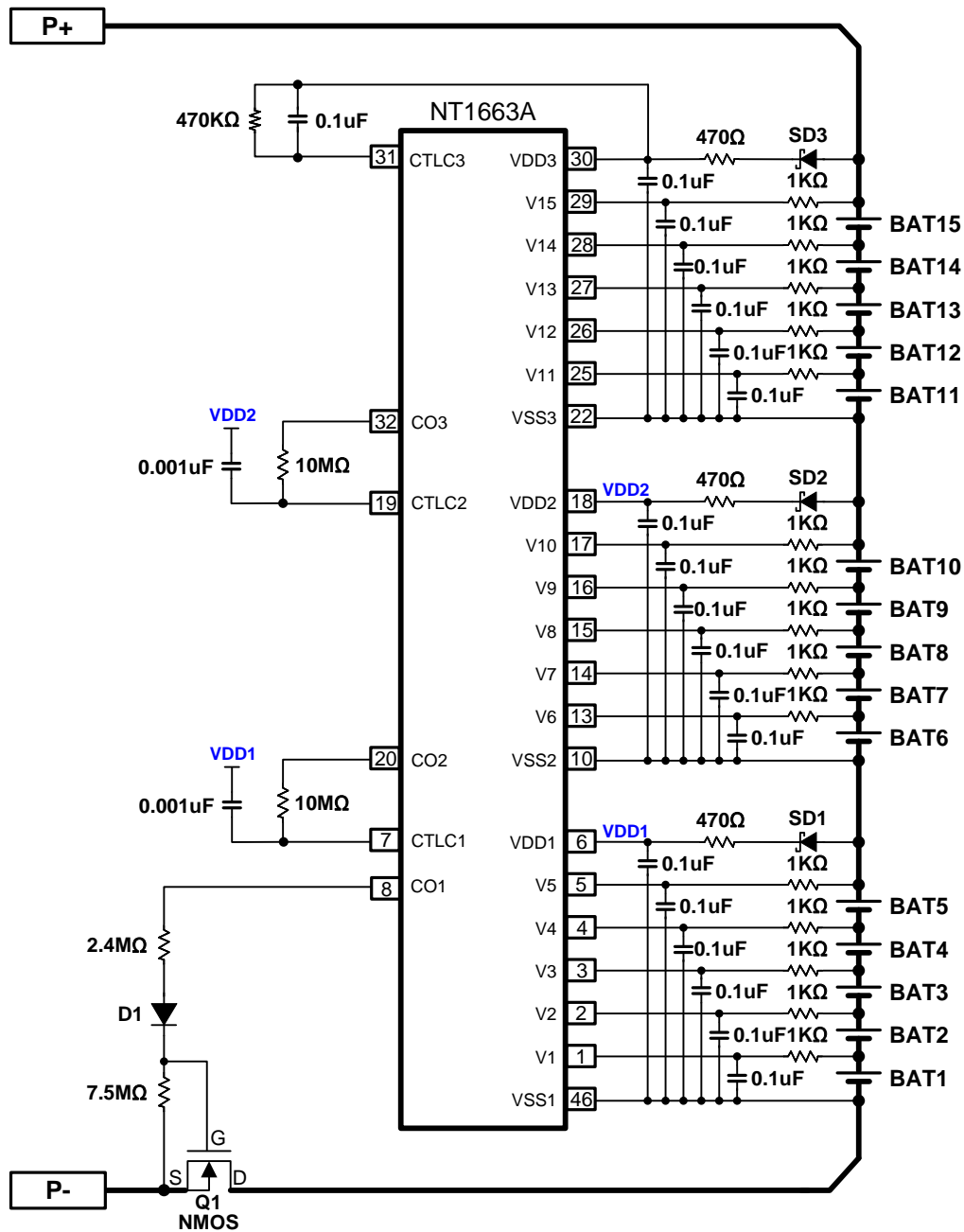
- NT1660A



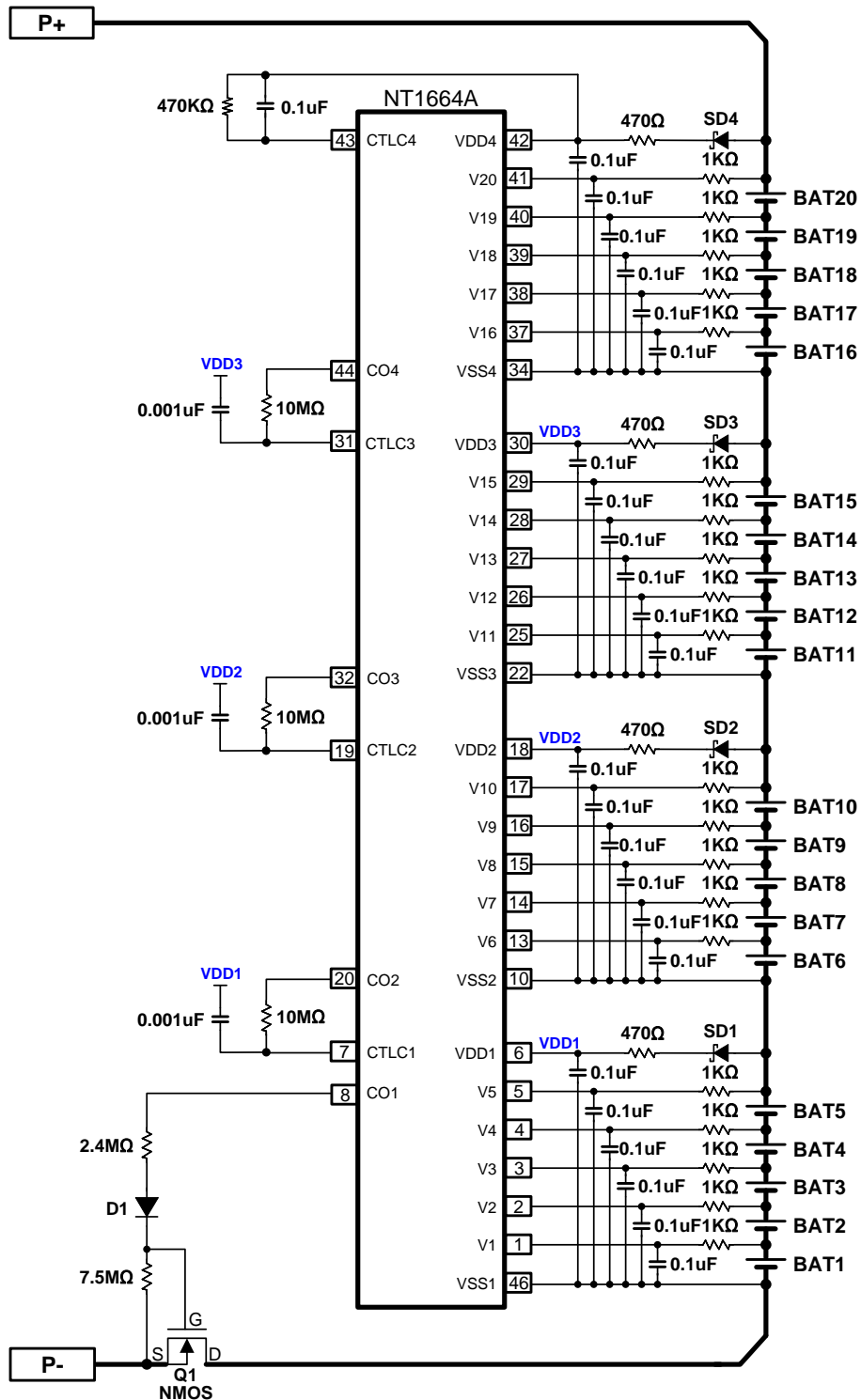
These devices have limited build-in ESD protection. The leads must be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

■ NT1662A


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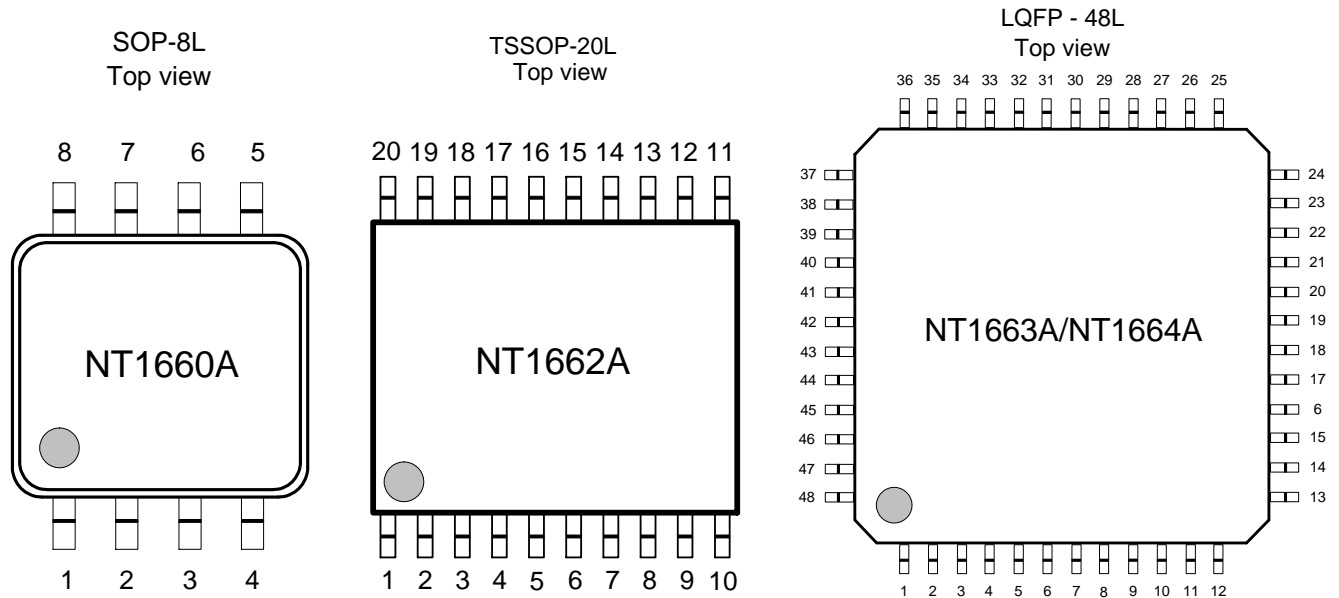
■ NT1663A


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Package and Pin Configurations



Pin No				Symbol	Pin description
NT1660A	NT1662A	NT1663A	NT1664A		
1	-	-	-	VDD	Power supply input pin
-	3	6	6	VDD1	Power supply input pin -1
-	13	18	18	VDD2	Power supply input pin -2
-	-	30	30	VDD3	Power supply input pin -3
-	-	-	42	VDD4	Power supply input pin -4
3	-	-	-	VSS	Reference voltage
-	17	46	46	VSS1	Reference voltage -1
-	7	10	10	VSS2	Reference voltage -2
-	-	22	22	VSS3	Reference voltage -3
-	-	-	34	VSS4	Reference voltage -4

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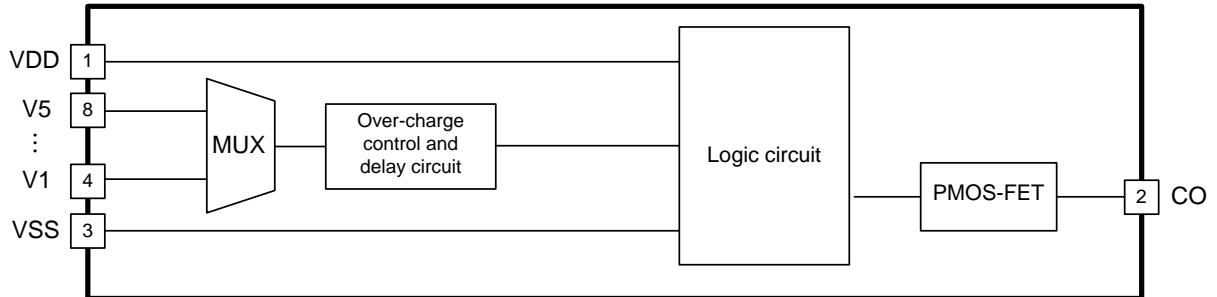
Pin No				Symbol	Pin description
NT1660A	NT1662A	NT1663A	NT1664A		
4	18	1	1	V1	Cell BAT1 positive voltage and cell BAT2 negative voltage input pin.
5	19	2	2	V2	Cell BAT2 positive voltage and cell BAT3 negative voltage input pin.
6	20	3	3	V3	Cell BAT3 positive voltage and cell BAT4 negative voltage input pin.
7	1	4	4	V4	Cell BAT4 positive voltage and cell BAT5 negative voltage input pin.
8	2	5	5	V5	Cell BAT5 positive voltage and cell BAT6 negative voltage input pin.
-	8	13	13	V6	Cell BAT6 positive voltage and cell BAT7 negative voltage input pin.
-	9	14	14	V7	Cell BAT7 positive voltage and cell BAT8 negative voltage input pin.
-	10	15	15	V8	Cell BAT8 positive voltage and cell BAT9 negative voltage input pin.
-	11	16	16	V9	Cell BAT9 positive voltage and cell BAT10 negative voltage input pin.
-	12	17	17	V10	Cell BAT10 positive voltage and cell BAT11 negative voltage input pin.
-	-	25	25	V11	Cell BAT11 positive voltage and cell BAT12 negative voltage input pin.
-	-	26	26	V12	Cell BAT12 positive voltage and cell BAT13 negative voltage input pin.
-	-	27	27	V13	Cell BAT13 positive voltage and cell BAT14 negative voltage input pin.
-	-	28	28	V14	Cell BAT14 positive voltage and cell BAT15 negative voltage input pin.
-	-	29	19	V15	Cell BAT15 positive voltage and cell BAT16 negative voltage input pin.
-	-	-	37	V16	Cell BAT16 positive voltage and cell BAT17 negative voltage input pin.
-	-	-	38	V17	Cell BAT17 positive voltage and cell BAT18 negative voltage input pin.
-	-	-	39	V18	Cell BAT18 positive voltage and cell BAT19 negative voltage input pin.
-	-	-	40	V19	Cell BAT19 positive voltage and cell BAT20 negative voltage input pin.
-	-	-	41	V20	Cell BAT20 positive voltage.

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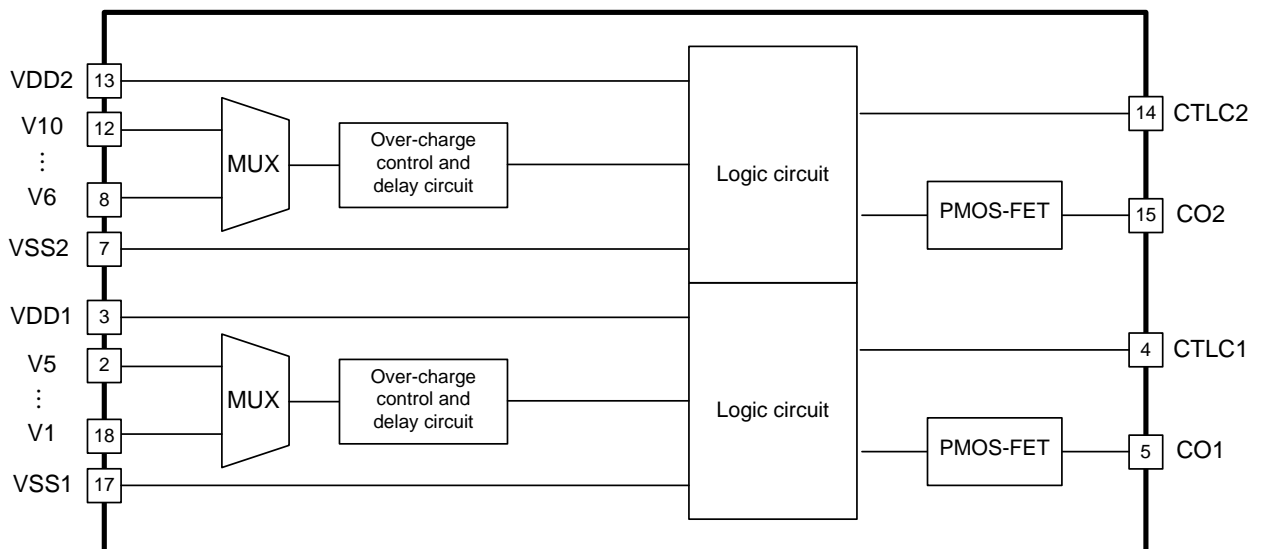
Pin No.				Symbol	Pin description
NT1660A	NT1662A	NT1663A	NT1664A		
2	-	-	-	CO	FET gate control pin for charging path (Pch open-drain output). ● Normal mode : High ● Overcharge mode : Hi-impedance
-	5	8	8	CO1	FET gate control pin for charging path -1 (Pch open-drain output). ● Normal mode : High ● Overcharge mode : Hi-impedance
-	15	20	20	CO2	FET gate control pin for charging path -2 (Pch open-drain output). ● Normal mode : High ● Overcharge mode : Hi-impedance
-	-	32	32	CO3	FET gate control pin for charging path -3 (Pch open-drain output). ● Normal mode : High ● Overcharge mode : Hi-impedance
-	-	-	44	CO4	FET gate control pin for charging path -4 (Pch open-drain output). ● Normal mode : High ● Overcharge mode : Hi-impedance
-	-	-	-	CTLC	The control terminal of output overcharge detection ● $I_{CTLC} > I_{CTLCH}$ CO pin : Normal mode ● $I_{CTLC} < I_{CTLCL}$ CO pin : Hi-impedance
-	4	7	7	CTLC1	The control terminal of output overcharge detection -1. ● $I_{CTLC} > I_{CTLCH}$ CO pin : Normal mode ● $I_{CTLC} < I_{CTLCL}$ CO pin : Hi-impedance
-	14	19	19	CTLC2	The control terminal of output overcharge detection -2. ● $I_{CTLC} > I_{CTLCH}$ CO pin : Normal mode ● $I_{CTLC} < I_{CTLCL}$ CO pin : Hi-impedance
-	-	31	31	CTLC3	The control terminal of output overcharge detection -3. ● $I_{CTLC} > I_{CTLCH}$ CO pin : Normal mode ● $I_{CTLC} < I_{CTLCL}$ CO pin : Hi-impedance
-	-	-	43	CTLC4	The control terminal of output overcharge detection -4. ● $I_{CTLC} > I_{CTLCH}$ CO pin : Normal mode ● $I_{CTLC} < I_{CTLCL}$ CO pin : Hi-impedance
-	6,16	9,11,12,21,23,24,33-45,47,48	9,11,12,21,23,24,33,35,36,45,47,48	N/C	No Connect. (Floating)

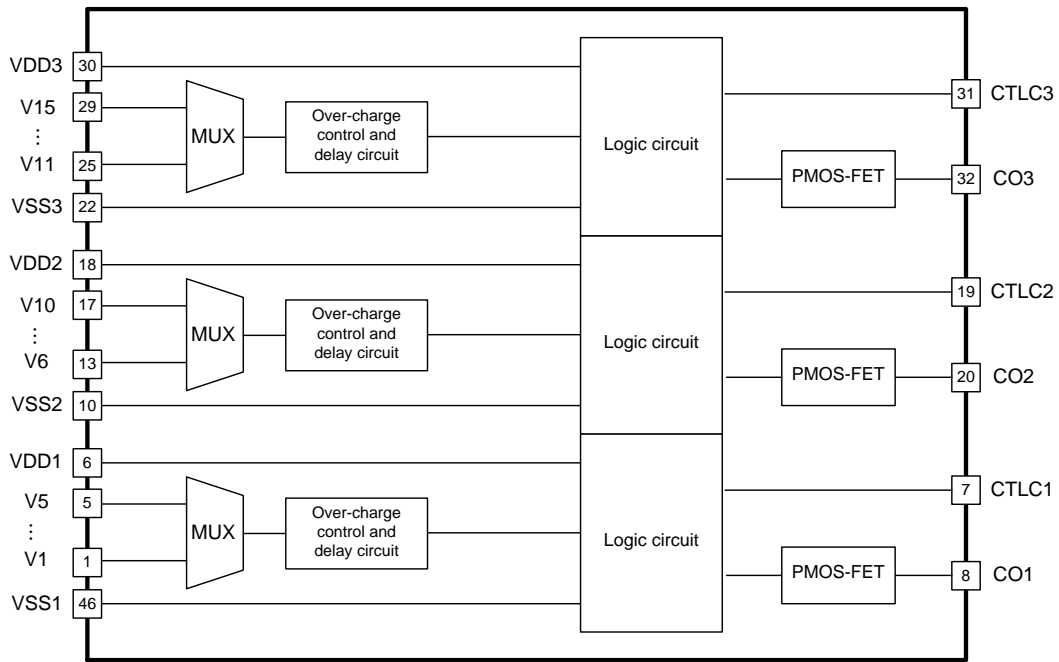
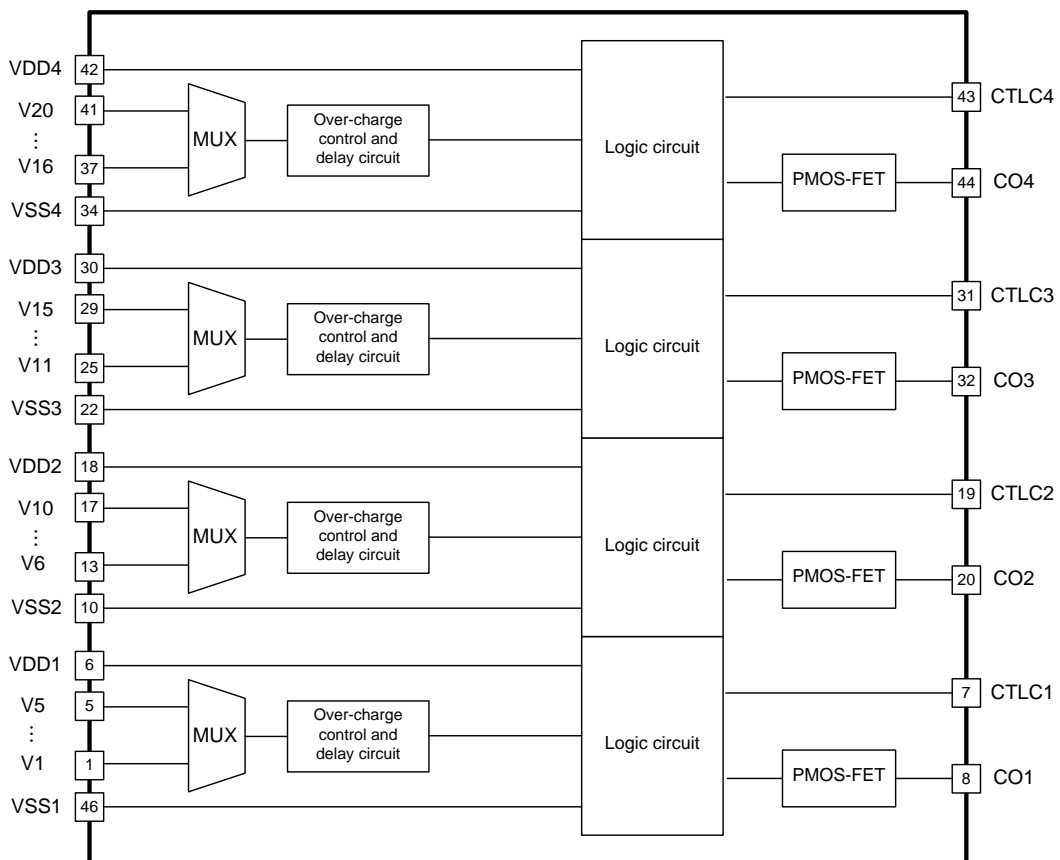
Block Diagram

■ NT1660A



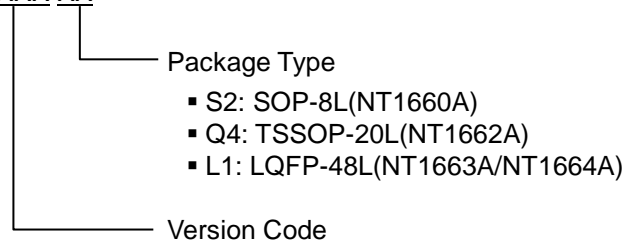
■ NT1662A



■ NT1663A

■ NT1664A


Ordering Information

NT166xA(x=0,2,3,4)-XXX XX



Product version code:

Table 1: Detection threshold level

Product Name	Version Code	Package Type	Over-charge detection voltage V_{DET1} (V)	Over-charge release voltage V_{REL1} (V)	Overcharge detection delay time t_{VDET1} (s) $\pm 30\%$	Overcharge release condition	Built-in breaking wire detector function
NT1660A	F1A	S2	4.250	4.150	1	Voltage release	Yes
NT1660A	J1A	S2	4.300	4.200	1		
NT1662A	F1A	Q4	4.250	4.150	1		
NT1662A	J1A	Q4	4.300	4.200	1		
NT1663A	F1A	L1	4.250	4.150	1		
NT1663A	J1A	L1	4.300	4.200	1		
NT1664A	F1A	L1	4.250	4.150	1		
NT1664A	J1A	L1	4.300	4.200	1		