NT7107C

INTRODUCTION

The NT7107 is a LCD driver LSI with 64 channel outputs for dot matrix liquid crystal graphic display systems. This device provides 64 shift registers and 64 output drivers. It generates the timing signal to control the NT7108.

The NT7107 is fabricated by low power CMOS high voltage process technology, and is composed of the liquid crystal display system in combination with the NT7108 (64 channel segment driver).

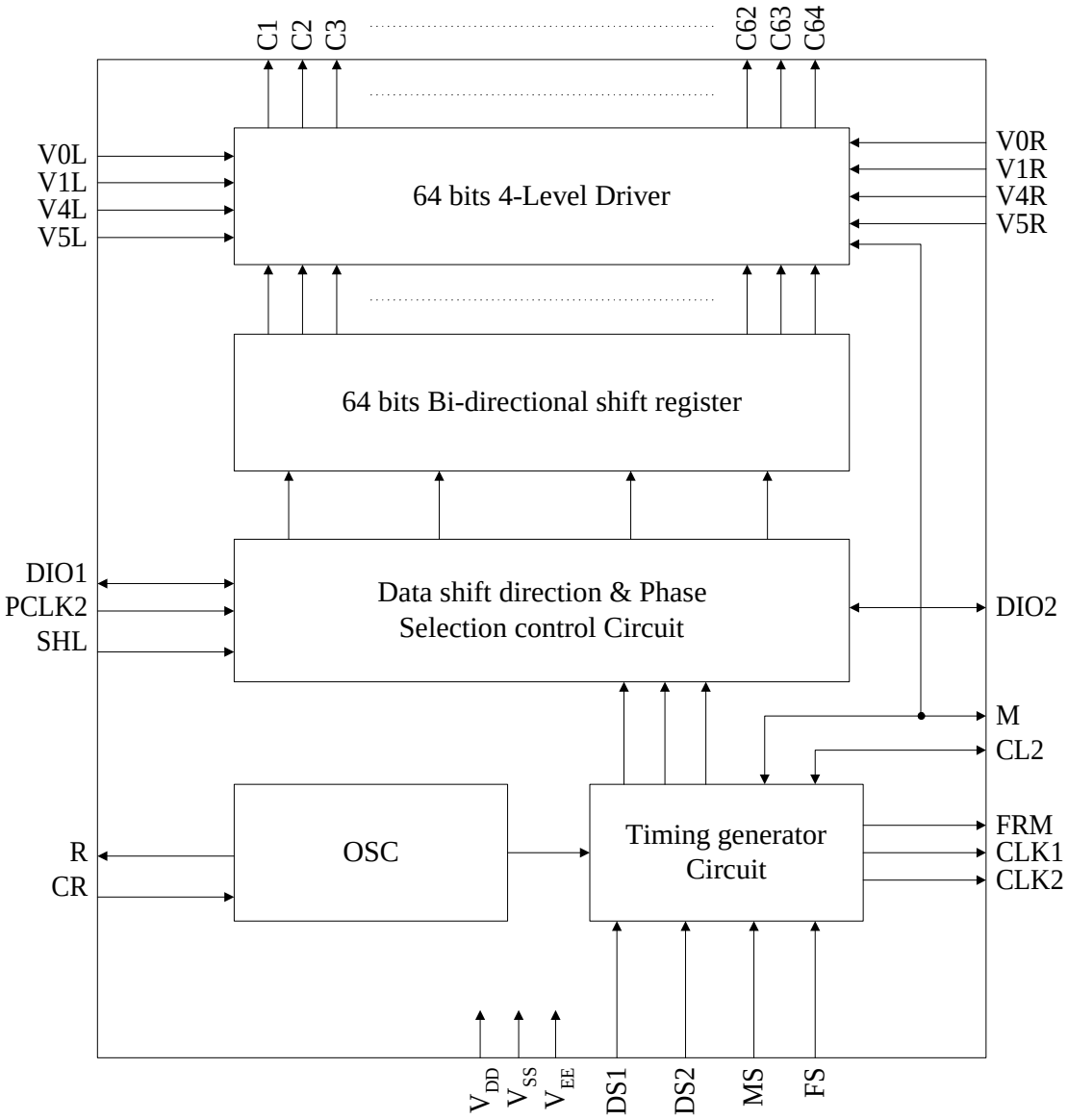
FEATURES

- Dot matrix LCD common driver with 64 channel output
- 64-bit shift register at internal LCD driver circuit
- Internal timing generator circuit for dynamic display
- Selection of master/slave mode
- Applicable LCD duty: 1/48, 1/64, 1/96, 1/128
- Power supply voltage:+2.7~+5.5V
- LCD driving voltage: 8V~17V (V_{DD}-V_{EE})
- Interface

Driver		**Controller**
COMMON	SEGMENT	
Other NT7107	Other NT7108	MPU

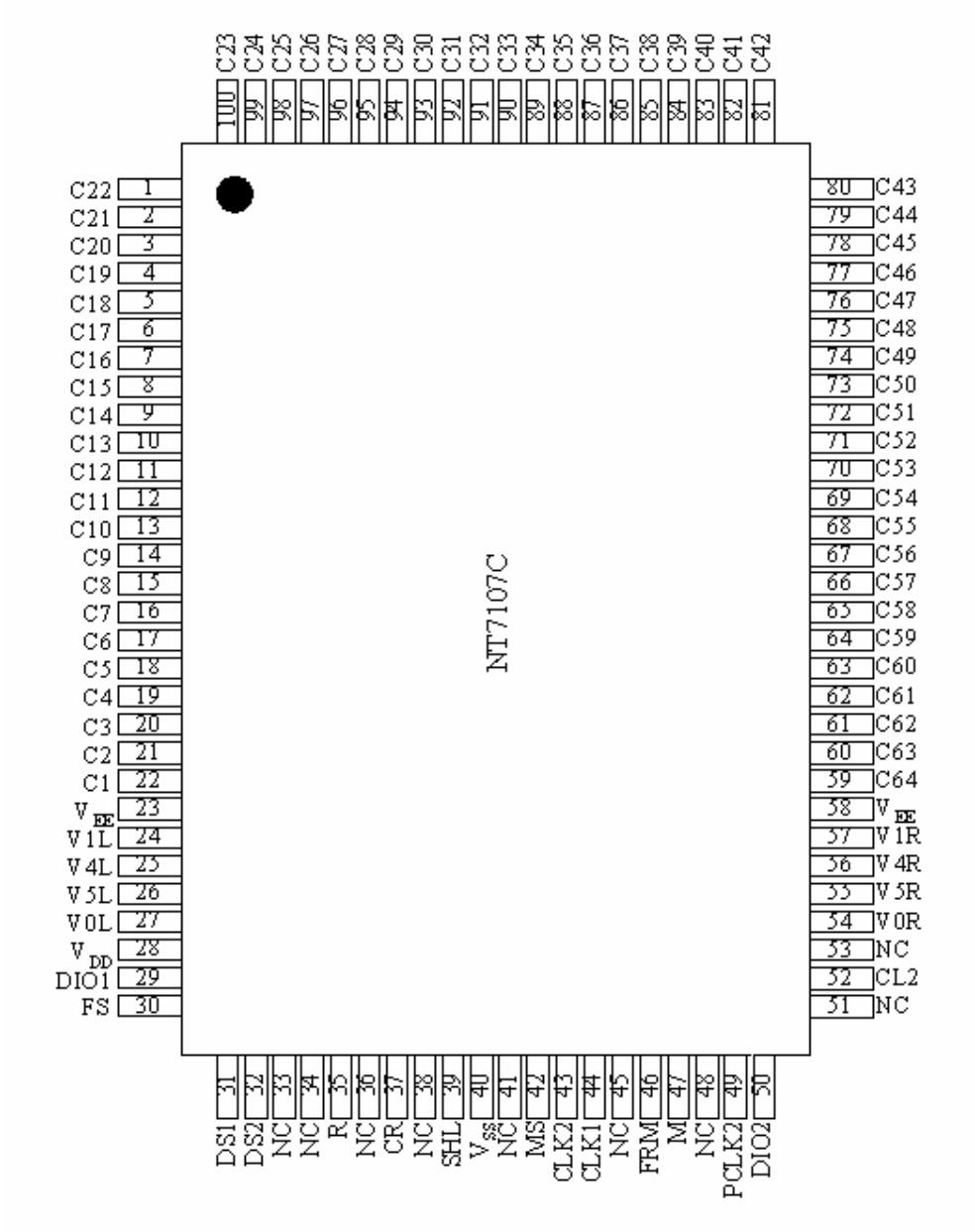
- High voltage CMOS process
- Bare chip, LQFP 100L, QFP 100L available

BLOCK DIAGRAM

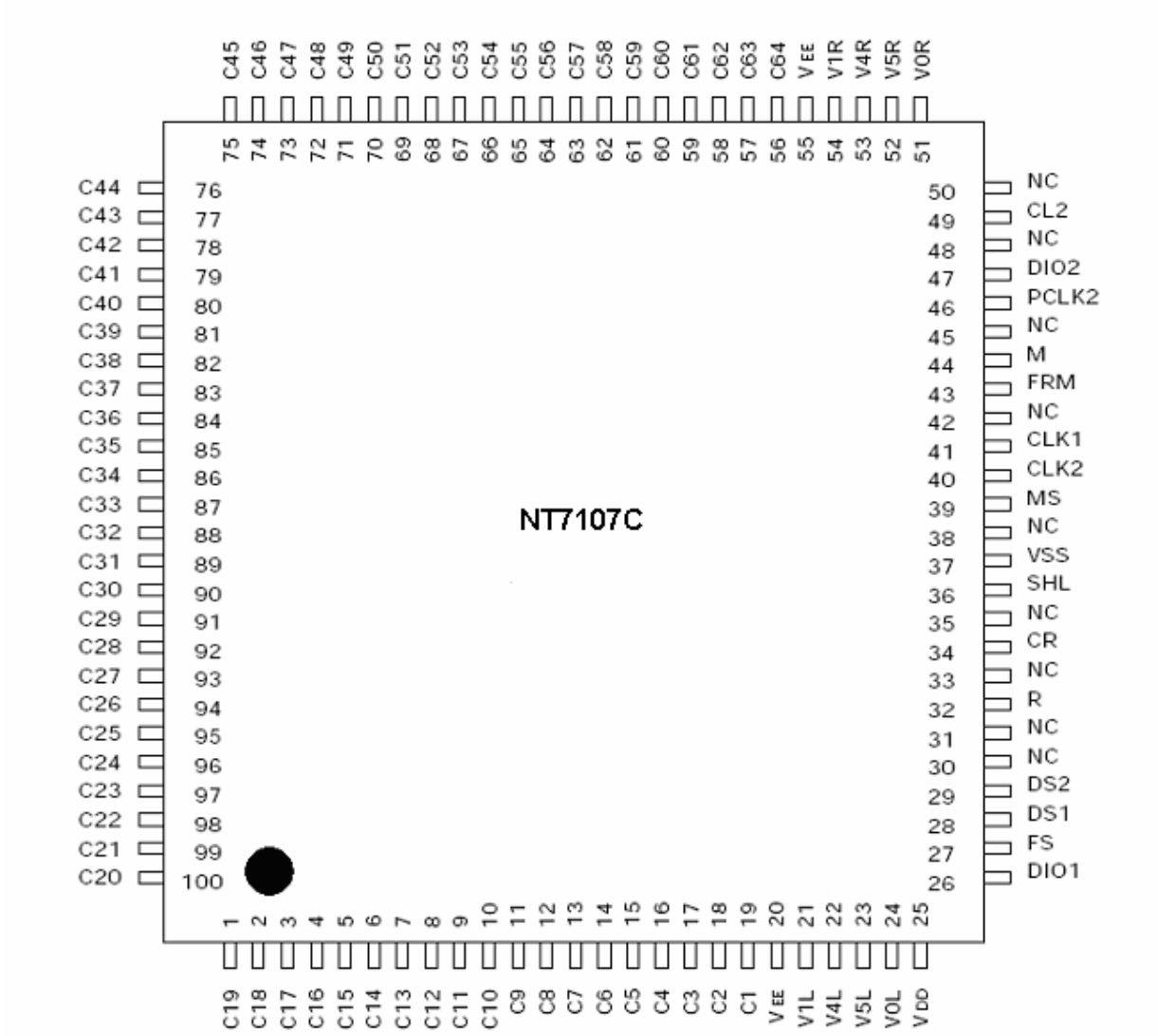


PIN CONFIGULATION

QFP 100L PACKAGE



LQFP 100L PACKAGE

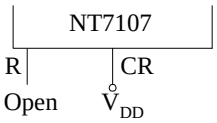


PIN DESCIPTION

Table 1. Pin Description

<table>
<tr><th>Pin Number
QFP</th><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>28</td><td>V_{DD}</td><td rowspan="3">Power</td><td>For internal logic circuit (+2.7~+5.5V)</td></tr>
<tr><td>40</td><td>V_{SS}</td><td>GND (=0V)</td></tr>
<tr><td>23,58</td><td>V_{EE}</td><td>For LCD driver circuit</td></tr>
<tr><td>27,54
24,57
25,56
26,55</td><td>V0L,V0R
V1L,V1R
V4L,V4R
V5L,V5R</td><td>Power</td><td>Bias supply voltage terminals to drive LCD.
<table><tr><th>Select Level</th><th>Non-Select Level</th></tr><tr><td>V0L I, V5L I</td><td>V1L I, V4L I</td></tr></table>The same voltage should connect V0L and V0R (V1L & V1R, V4L & V4R, V5L & V5R).</td></tr>
<tr><td>42</td><td>MS</td><td>Input</td><td>Section of master/slave mode
· Master mode (MS=1)
DlO1, DlO2, CL2 and M is output state.
· Salve mode (MS=0)
SHL=1 DlO1 is input state (DlO2 is output state)
SHL=0 DlO2 is input state (DlO1 is output state)
CL2 and M are input state.</td></tr>
<tr><td>39</td><td>SHL</td><td>Input</td><td>Selection of data shift direction.
<table><tr><th>SHL</th><th>Data Shift Direction</th></tr><tr><td>H</td><td>DlO1 C1....C64 DlO2</td></tr><tr><td>L</td><td>DlO2 C64....C1 DlO1</td></tr></table></td></tr>
<tr><td>49</td><td>PCLK2</td><td>Input</td><td>Selection of shift clock (CL2) phase.
<table><tr><th>PCLK2</th><th>Data Clock (CL2) Phase</th></tr><tr><td>H</td><td>Data shift at the rising edge of CL2</td></tr><tr><td>L</td><td>Data shift at the falling edge of CL2</td></tr></table></td></tr>
<tr><td>30</td><td>FS</td><td>Input</td><td>Selection of oscillation frequency.
· Master mode
when the frame frequency is 70 Hz, the oscillation frequency should be
fosc=430kHz at FS=1(V_{DD})
fosc=215kHz at FS=0(Vss)
· Slave mode
Connect to V_{DD}</td></tr>
<tr><td>31
32</td><td>DS1
DS2</td><td>Input</td><td>Selection of display duty.
· Master mode
<table><tr><th>DS1</th><th>DS2</th><th>Duty</th></tr><tr><td rowspan="2">L</td><td>L</td><td>1/48</td></tr><tr><td>H</td><td>1/64</td></tr><tr><td rowspan="2">H</td><td>L</td><td>1/96</td></tr><tr><td>H</td><td>1/128</td></tr></table>· Slave mode: Connect to VDD.</td></tr>
</table>

<table>
<tr><th>Pin Number
QFP</th><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>35
37</td><td>R
CR</td><td></td><td>RC Oscillator (Built-in capacitor)
· Master mode: Use these terminals as shown below.
 

· Slave mode: Stop the oscillator as shown below.
 
</td></tr>
<tr><td>44
43</td><td>CLK1
CLK2</td><td>Output</td><td>Operating clock output for the NT7108
· Master mode: connection to CLK1 and CLK2 of the NT7108
· Slave mode: open</td></tr>
<tr><td>46</td><td>FRM</td><td>Output</td><td>Synchronous frame signal.
· Master mode: connection to FRM of the NT7108
· Slave mode: open</td></tr>
<tr><td>47</td><td>M</td><td>Input/
Output</td><td>Alternating signal input for LCD driving.
· Master mode: output state Connection to M of the NT7108
· Slave mode: input state Connection to the controller</td></tr>
<tr><td>52</td><td>CL2</td><td>Input/
Output</td><td>Data shift clock
· Master mode: output state Connection to CL of the NT7108
· Slave mode: input state connection to shift clock terminal of the controller.</td></tr>
<tr><td>29
50</td><td>DIO1
DIO2</td><td>Input/
Output</td><td>Data input/output pins of internal shift register.
<table>
<tr><th>MS</th><th>SHL</th><th>DIO1</th><th>DIO2</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>Output</td><td>Output</td></tr>
<tr><td>L</td><td>Output</td><td>Output</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>Input</td><td>Output</td></tr>
<tr><td>L</td><td>Output</td><td>Input</td></tr>
</table></td></tr>
<tr><td>22-1
100-59</td><td>C1-C64</td><td>Output</td><td>Common signal output for LCD driving.
<table>
<tr><th>Data</th><th>M</th><th>Out</th></tr>
<tr><td rowspan="2">L</td><td>L</td><td>V1</td></tr>
<tr><td>H</td><td>V4</td></tr>
<tr><td rowspan="2">H</td><td>L</td><td>V5</td></tr>
<tr><td>H</td><td>V0</td></tr>
</table></td></tr>
<tr><td>33,34,36
38,41,45
48,51,53</td><td>NC</td><td></td><td>No connection</td></tr>
</table>

MAXIMUM ABSOLUTE LIMIT

Characteristic	Symbol	Value	Unit	Note
Operating voltage	V_{DD}	-0.3 to +7.0	V	(1)
Supply voltage	V_{EE}	V_{DD}-19.0 to VDD+0.3		(4)
Driver supply voltage	V_B	-0.3 to V_{DD}+0.3		(1),(2)
	V_{LCD}	V_{EE}-0.3 to V_{DD}+0.3		(3),(4)
Operating temperature	T_{OPR}	-30 to +85	℃	-
Storage temperature	T_{STG}	-55 to +125		-

NOTES:

1. Based on Vss=0V
2. Applies to input terminals and I/O terminals at high impedance. (Except V0LI, V1LI, V4LI and V5LI)
3. Applies to V0LI, V1LI, V4LI and V5LI.
4. Voltage level: $V_{DD} \geqq V0L=V0R \geqq V1L=V1R \geqq V4L=V4R \geqq V5L=V5R \geqq V_{EE}$.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (V_{DD}=+5.0V, Vss=0V, |V_{DD}-V_{EE}|=8~17V, TA=-30 ~+85℃)

Characteristic		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating voltage		V_{DD}	-	2.7	-	5.5	V	
Input Voltage	High	V_{IH}	-	0.7V_{DD}	-	V_{DD}		(1)
	Low	V_{IL}	-	V_{SS}	-	0.3V_{DD}		
Output Voltage	High	V_{OH}	I_{OH}=-0.4mA	V_{DD}-0.4	-	-		(2)
	Low	V_{OL}	I_{OL}=0.4mA	-	-	0.4		
Input leakage current		I_{LKG}	$V_{IN}=V_{DD}-V_{SS}$	-1.0	-	1.0	μA	(1)
OSC frequency		f_{OSC}	Rf=47KΩ±2%	315	450	585	kHz	
On resistance (V_{DIV} – C_i)		R_{ON}	V_{DD}-V_{EE}=17V Load current = ±150 μA	-	-	1.5	KΩ	
Operating current		I_{DD1}	Master mode; 1/128duty	-	-	1.0	mA	(3)
		I_{DD2}	Slave mode; 1/128 duty	-	-	200	μA	(4)
Supply current		I_{EE}	Master mode; 1/128 duty	-	-	100		(5)
Operating Frequency		f_{OP1}	Master mode; External clock	50	-	600	kHz	
		f_{OP2}	Slave mode	0.5	-	1500		

NOTES:

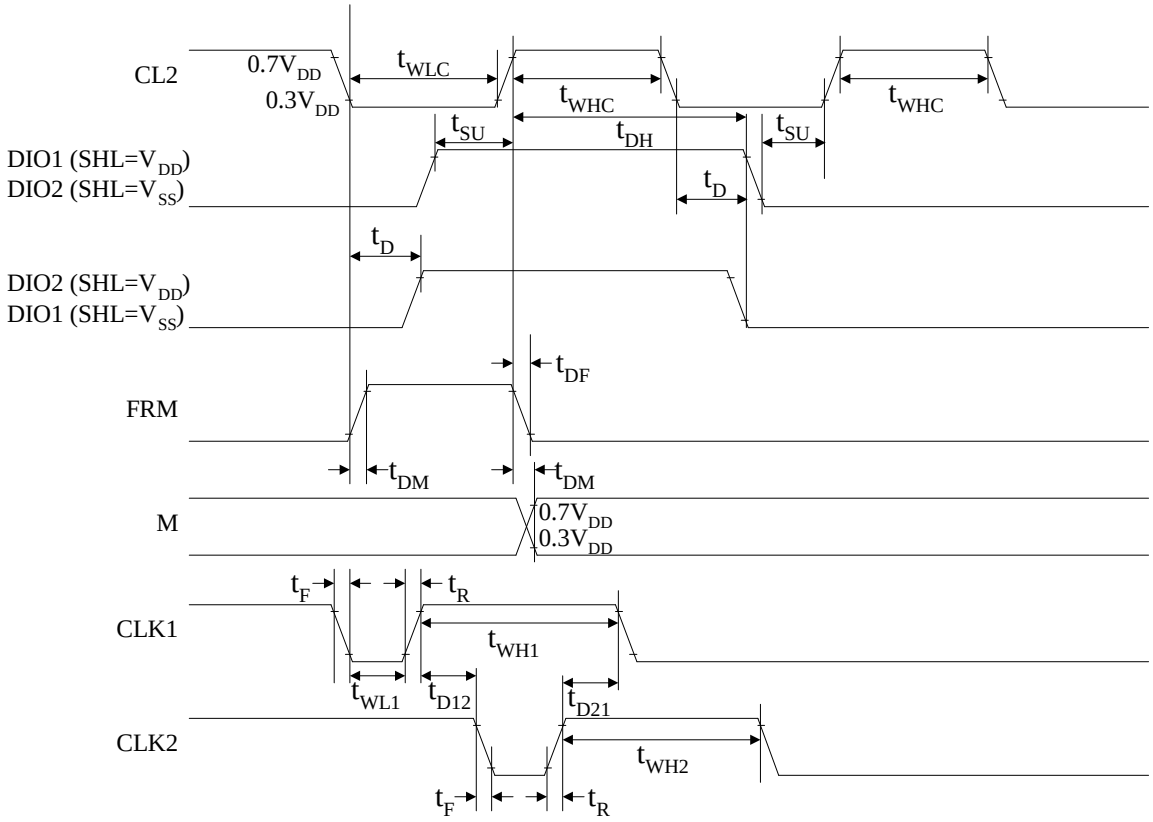
1. Applies to input terminals FS, DS1, DS2, CR, SHL, MS and PCLK2 and I/O terminals DIO1, DIO2, M and CL2 in the input state.
2. Applies to output terminals CLK1, CLK2 and FRM and I/O terminals DIO1, DIO2, M and CL2 in the Output State.
3. This value is specified at about the current flowing through Vss. Internal oscillation circuit: Rf = 47kΩ, Each terminal of DS1, DS2, FS, SHL and MS is connected to V_{DD} and out is no load.
4. This value is specified at about the current flowing through Vss. Each terminal of DS1, DS2, FS, SHL, PCLK2 and CR is connected to V_{DD}, and MS is connected to Vss. CL2, M, DIO1 is external

clock.

5. This value is specified at the current flowing through V_{EE}. Don connect to V_{LCD} (V1-V5).

AC CHARACTERISTICS (V_{DD}=5V±10%, TA=-30 ~+85℃)

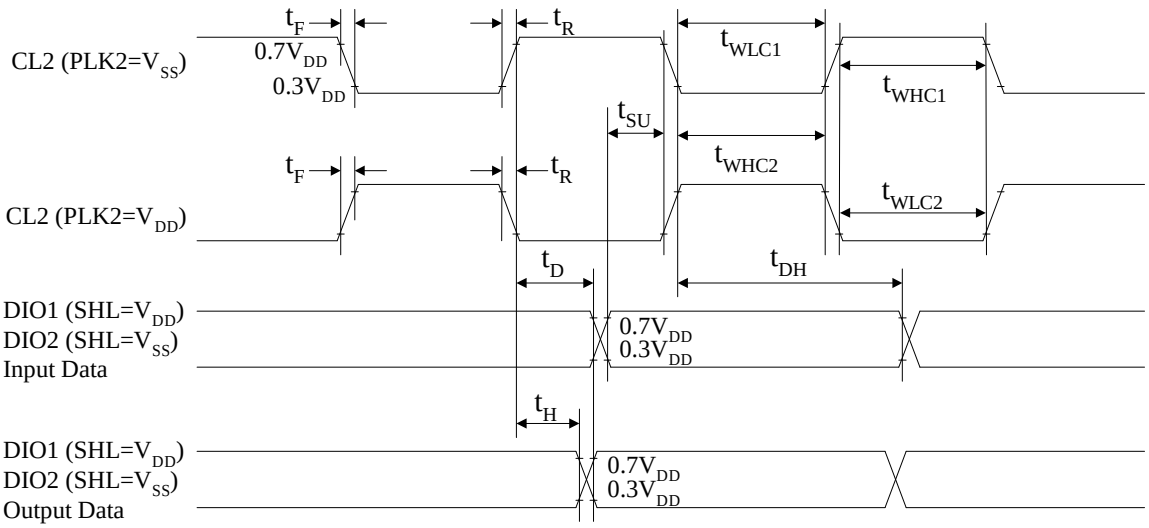
Master Mode (MS=V_{DD}, PCLK2=V_{DD})



Master Mode

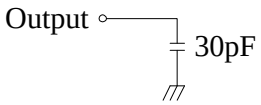
Characteristic	Symbol	Min.	Typ.	Max.	Unit
Data setup time	t_{SU}	20	-	-	μs
Data hold time	t_{DH}	40	-	-	
Data delay time	t_D	5	-	-	
FRM delay time	t_{DF}	-2	-	2	
M delay time	t_{DM}	-2	-	2	
CL2 low level width	t_{WLC}	35	-	-	
CL2 high level width	t_{WHC}	35	-	-	
CLK1 low level width	t_{WL1}	700	-	-	ns
CLK2 low level width	t_{WL2}	700	-	-	
CLK1 high level width	t_{WH1}	2100	-	-	
CLK2 high level width	t_{WH2}	2100	-	-	
CLK1-CLK2 phase difference	t_{D12}	700	-	-	
CLK2-CLK1 phase difference	t_{D21}	700	-	-	
CLK1,CLK2 rise/fall time	t_R/ t_F	-	-	150	

Slave Mode (MS=V_{SS})



Characteristic	Symbol	Min.	Typ.	Max.	Unit	Note
CL2 low level width	t_{WLC1}	450	-	-	ns	PCLK2=V_{SS}
CL2 high level width	t_{WHC1}	150	-	-		PCLK2=V_{SS}
CL2 low level width	t_{WLC2}	150	-	-		PCLK2=V_{DD}
CL2 high level width	t_{WHC2}	450	-	-		PCLK2=V_{DD}
Data setup time	t_{SU}	100	-	-		
Date hold time	t_{DH}	100	-	-		
Data delay time	t_D	-	-	200		(NOTE)
Output data hold time	t_H	10	-	-		
CL2 rise/fall time	t_R/ t_F	-	-	30		

NOTE: Connect load CL = 30pF

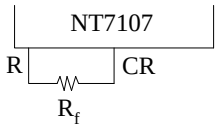


FUNCTIONAL DESCRIPTION

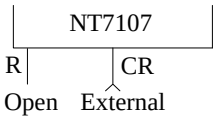
RC Oscillator

The RC Oscillator generates CL2, M, FRM of the NT7107, and CLK1 and CLK1 of the NT7108 by the oscillation resister R and internal capacitor C. When selecting the master/slave mode, the oscillation circuit is as following:

Master Mode: In the master mode, use these terminals as shown below.

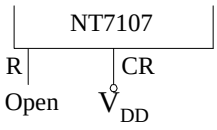


Internal Oscillation(Rf=47kΩ)



External Clock

Slave Mode: In the slave mode, stop the oscillator as shown below.



Timing Generation Circuit

It generates CL2, M, FRM, CLK1 and CLK2 by the frequency from the oscillation circuit.

Selection of Master/Slave (M/S) Mode

When MS is H, it generates CL2, M, FRM, CLK1 and CLK2 internally.

When MS is L, it operates by receiving M and CL2 from the master device.

Frequency Selection (FS)

To adjust FRM frequency by 70Hz, the oscillation frequency should be as follows:

FS	Oscillation Frequency
H	f_{OSC}=430kHz
L	f_{OSC}=215kHz

In the slave mode, it is connected to V_{DD}.

Duty Selection (DS1, DS2)

It provides various duty selections according to DS1 and DS2.

DS1	DS2	Duty
L	L	1/48
	H	1/64
H	L	1/96
	H	1/128

Data Shift & Phase Select Control

Phase Selection

It is a circuit to shift data on synchronization of rising edge, or falling edge of the CL2 according to PCLK2.

PCLK2	Phase Selection
H	Data shift on rising edge of CL2
L	Data shift on falling edge of CL2

Data shift Direction Selection

When MS is connected to V_{DD}, DIO1 and DIO2 terminal is only output.

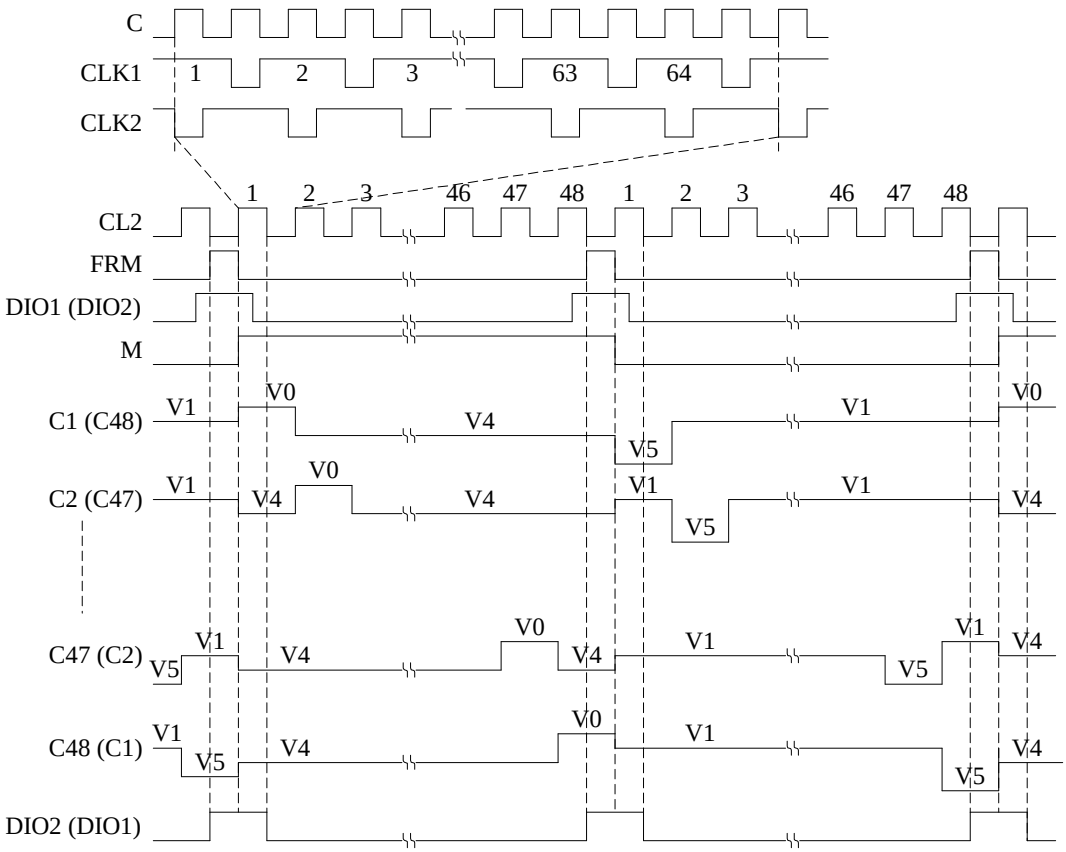
When MS is connected to Vss, it depends on the SHL.

MS	SHL	DIO1	DIO2	Direction of Data
H	H	Output	Output	C1 **à** C64
	L	Output	Output	C64 **à** C1
L	H	Input	Output	DIO1 **à** C1 **à** C64 **à** DIO2
	L	Output	Input	DIO2 **à** C64 **à** C1 **à** DIO1

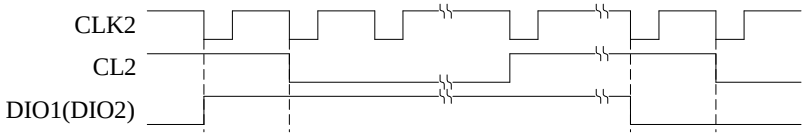
TIMING DIAGRAM

1/48 DUTY TIMING (MASTER MODE)

Condition: DS1=L, DS2=L, SHL=H (L), PCLK2=H

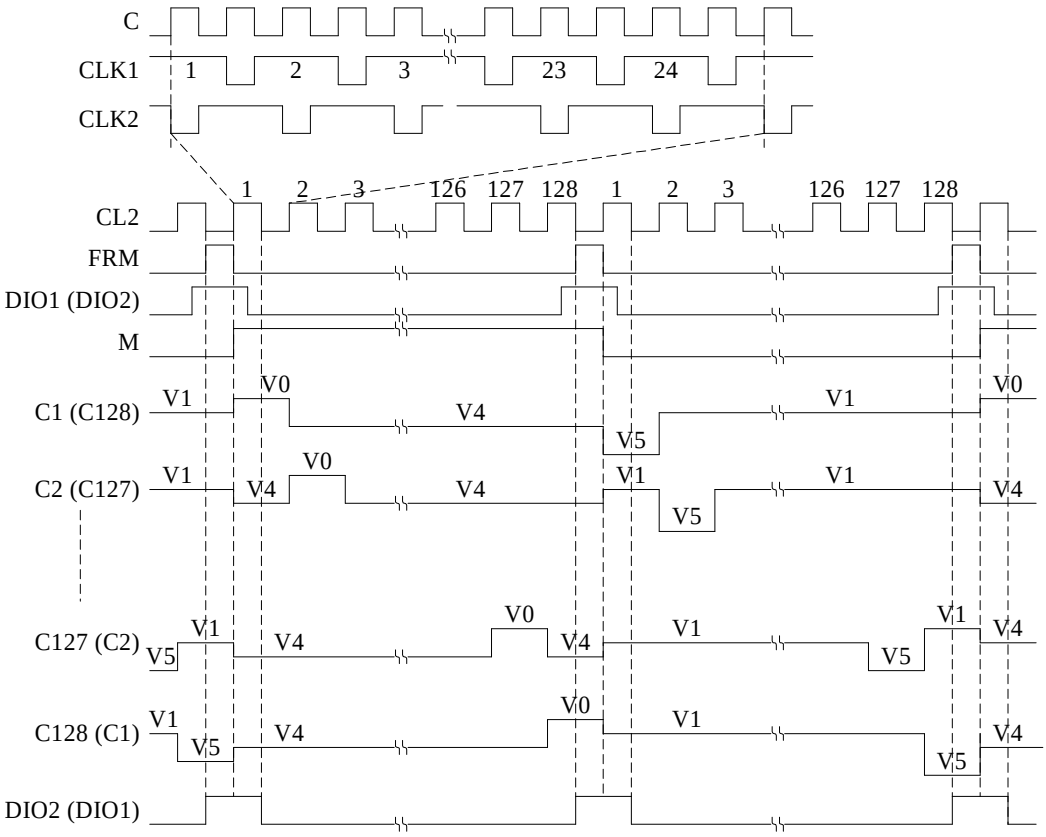


Relation of CL2 and DIO1(DIO2)

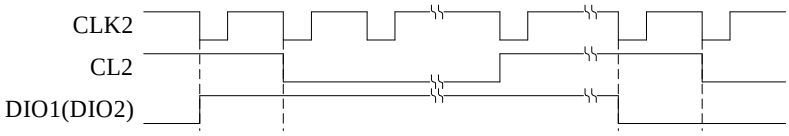


1/128 DUTY TIMING (MASTER MODE)

Condition: DS1=H, DS2=H, SHL=H(L), PCLK2=H

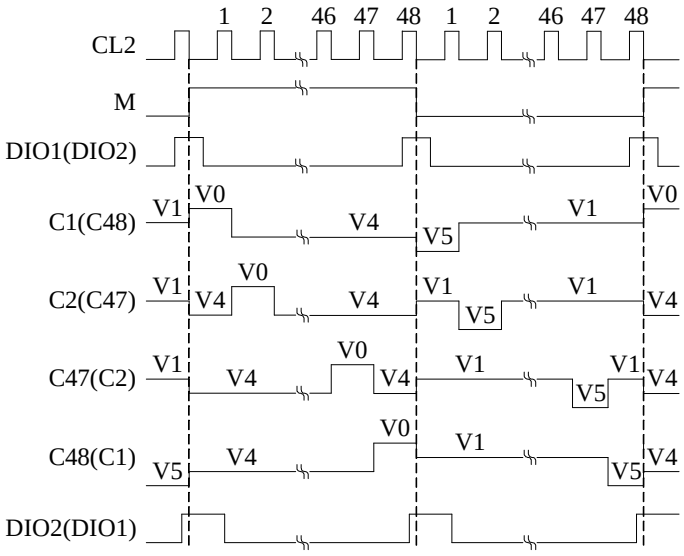


Relation of CL2 and DIO1(DIO2)

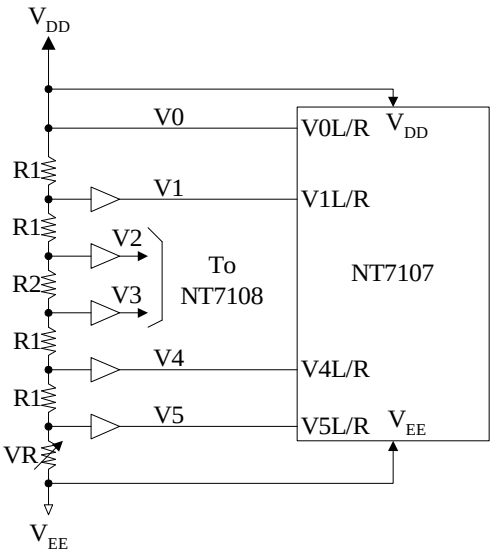


1/48 DUTY TIMING (SLAVE MODE)

Condition: SHL=H (L), PCLK2=L



POWER DRIVER CIRCUIT



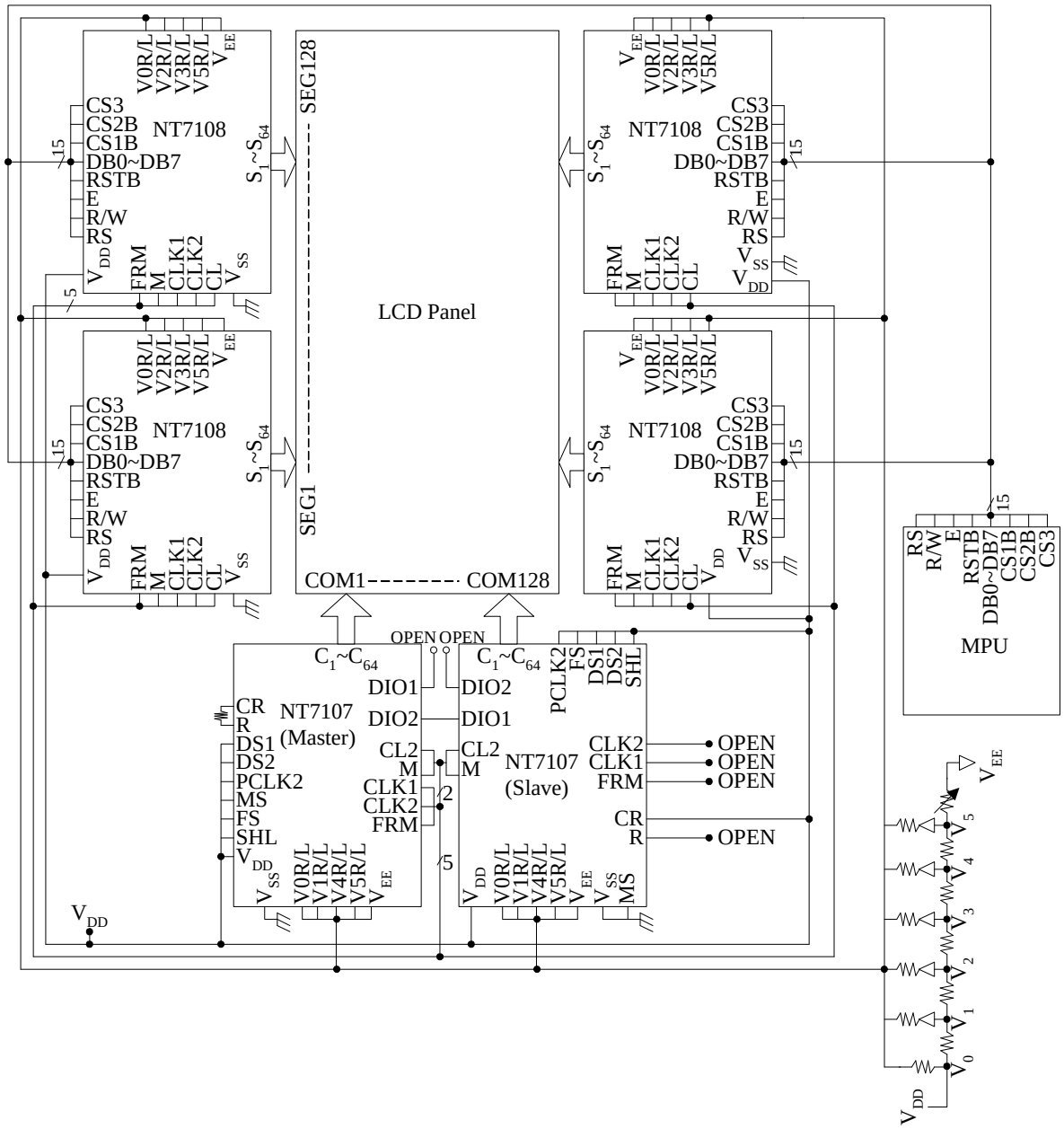
Relation of Duty & Bias

Duty	Bias	RDIV
1/48	1/8	R2=4R1
1/64	1/9	R2=5R1
1/96	1/11	R2=7R1
1/128	1/12	R2=8R1

When duty factor is 1/48, the value of R1 & R2 should satisfy.
R1/(4R1 + R2)=1/8 ;
R1=3kΩ , R2=12kΩ

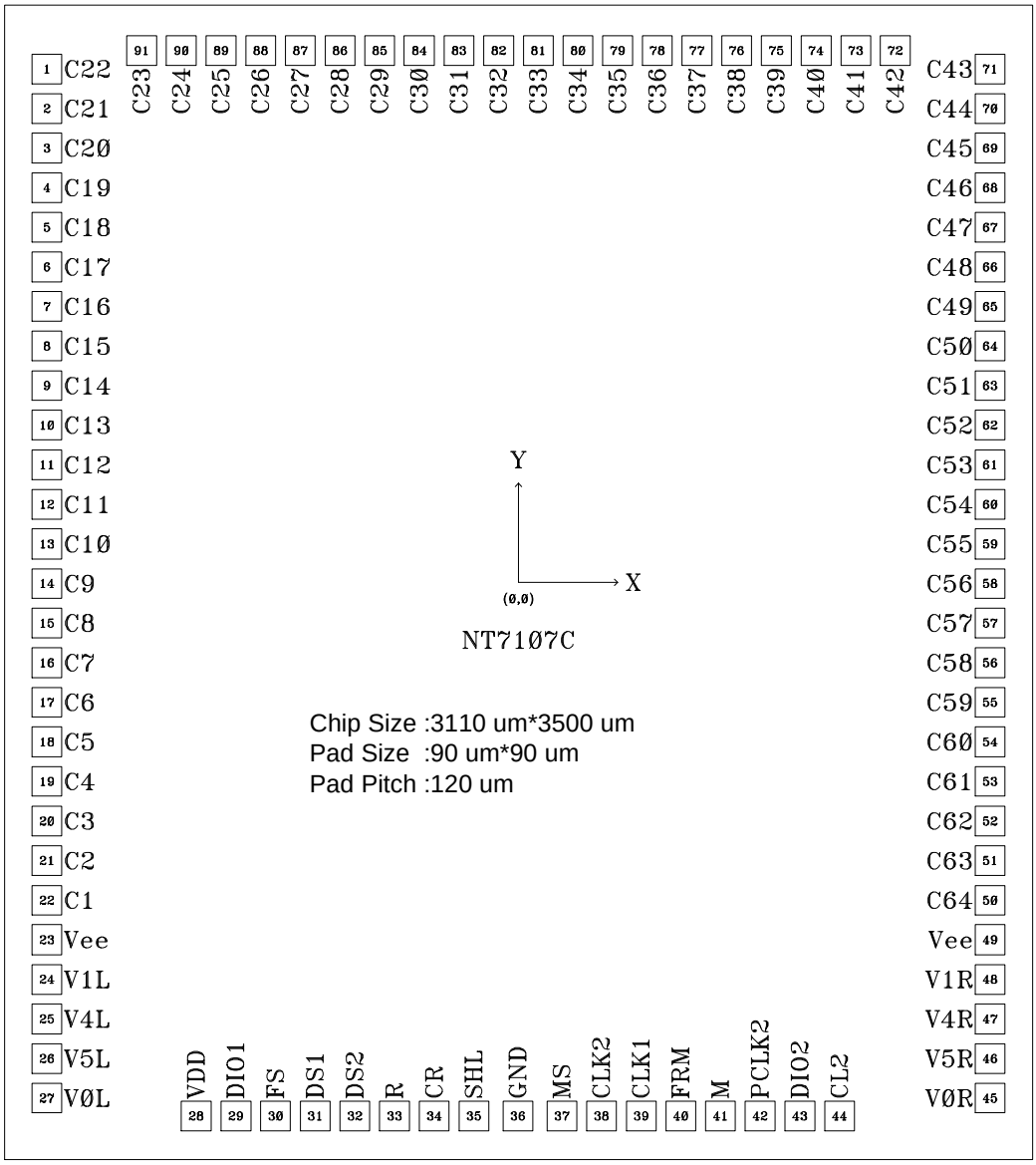
APPLICATION CIRCUIT

1/128 duty Segment driver (NT7108) interface circuit



PAD DIAGRAM

Note: Please connects the substrate to V_{DD} or floating.

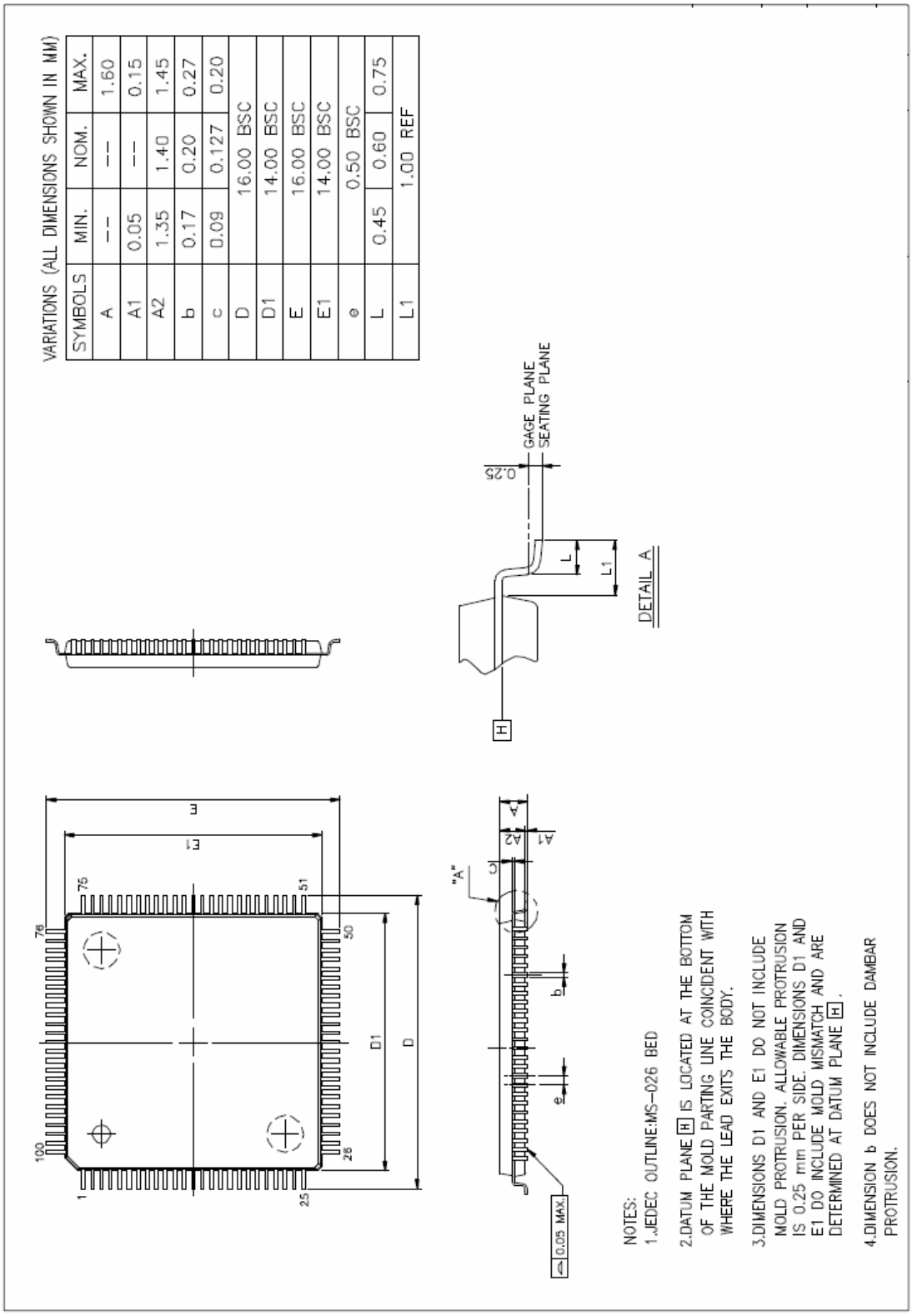


PAD DIAGRAM

PAD		COORDINATES	
NO.	NAME	X	Y
1	C22	-1426.70	1556.10
2	C21	-1426.70	1436.10
3	C20	-1426.70	1316.10
4	C19	-1426.70	1196.10
5	C18	-1426.70	1076.10
6	C17	-1426.70	956.10
7	C16	-1426.70	836.10
8	C15	-1426.70	716.10
9	C14	-1426.70	596.10
10	C13	-1426.70	476.10
11	C12	-1426.70	356.10
12	C11	-1426.70	236.10
13	C10	-1426.70	116.10
14	C9	-1426.70	-3.90
15	C8	-1426.70	-123.90
16	C7	-1426.70	-243.90
17	C6	-1426.70	-363.90
18	C5	-1426.70	-483.90
19	C4	-1426.70	-603.90
20	C3	-1426.70	-723.90
21	C2	-1426.70	-843.90
22	C1	-1426.70	-963.90
23	Vee	-1426.70	-1083.90
24	V1L	-1426.70	-1203.90
25	V4L	-1426.70	-1323.90
26	V5L	-1426.70	-1443.90
27	V0L	-1426.70	-1563.90
28	VDD	-974.90	-1618.10
29	DIO1	-854.90	-1618.10
30	FS	-734.90	-1618.10
31	DS1	-614.90	-1618.10
32	DS2	-494.90	-1618.10
33	R	-374.90	-1618.10
34	CR	-254.90	-1618.10
35	SHL	-134.90	-1618.10
36	GND	-1.90	-1618.10
37	MS	131.10	-1618.10
38	CLK2	251.10	-1618.10
39	CLK1	371.10	-1618.10
40	FRM	491.10	-1618.10
41	M	611.10	-1618.10
42	PCLK2	731.10	-1618.10
43	DIO2	851.10	-1618.10
44	CL2	971.10	-1618.10
45	V0R	1426.60	-1563.90
46	V5R	1426.60	-1443.90
47	V4R	1426.60	-1323.90

PAD		COORDINATES	
NO.	NAME	X	Y
48	V1R	1426.60	-1203.90
49	Vee	1426.60	-1083.90
50	C64	1426.60	-963.90
51	C63	1426.60	-843.90
52	C62	1426.60	-723.90
53	C61	1426.60	-603.90
54	C60	1426.60	-483.90
55	C59	1426.60	-363.90
56	C58	1426.60	-243.90
57	C57	1426.60	-123.90
58	C56	1426.60	-3.90
59	C55	1426.60	116.10
60	C54	1426.60	236.10
61	C53	1426.60	356.10
62	C52	1426.60	476.10
63	C51	1426.60	596.10
64	C50	1426.60	716.10
65	C49	1426.60	836.10
66	C48	1426.60	956.10
67	C47	1426.60	1076.10
68	C46	1426.60	1196.10
69	C45	1426.60	1316.10
70	C44	1426.60	1436.10
71	C43	1426.60	1556.10
72	C42	1140.00	1611.80
73	C41	1020.00	1611.80
74	C40	900.00	1611.80
75	C39	780.00	1611.80
76	C38	660.00	1611.80
77	C37	540.00	1611.80
78	C36	420.00	1611.80
79	C35	300.00	1611.80
80	C34	180.00	1611.80
81	C33	60.00	1611.80
82	C32	-60.00	1611.80
83	C31	-180.00	1611.80
84	C30	-300.00	1611.80
85	C29	-420.00	1611.80
86	C28	-540.00	1611.80
87	C27	-660.00	1611.80
88	C26	-780.00	1611.80
89	C25	-900.00	1611.80
90	C24	-1020.00	1611.80
91	C23	-1140.00	1611.80

LQFP 100L Outline Dimension

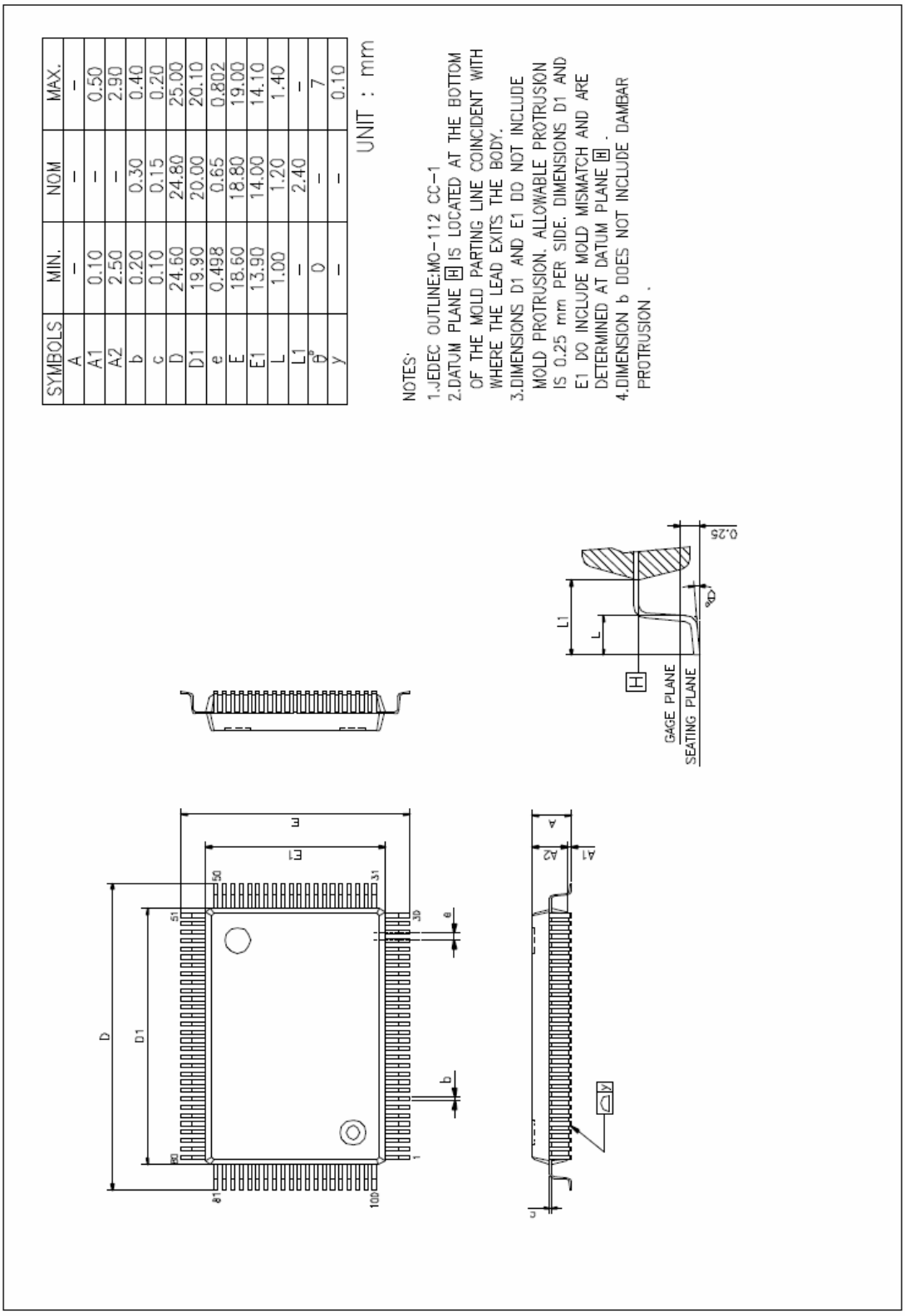


QFP 100L Outline Dimension

SYMBOLS	MIN.	NOM	MAX.
A	—	—	—
A1	0.10	—	0.50
A2	2.50	—	2.90
b	0.20	0.30	0.40
c	0.10	0.15	0.20
D	24.60	24.80	25.00
D1	19.90	20.00	20.10
e	0.498	0.65	0.802
E	18.60	18.80	19.00
E1	13.90	14.00	14.10
L	1.00	1.20	1.40
L1	—	2.40	—
θ°	0	—	7
y	—	—	0.10

UNIT : mm

NOTES:
1.JEDEC OUTLINE:MO-112 CC-1
2.DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H .
4.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION .



***Revision* History**

Ver. No	Date	Page	Description
0.11	2007/12/17	17	Modify Pad size description.
1.0	2015/08/17	19, 20	Add. LQFP, QFP outline dimension